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Lab 1 Notes

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CSE 2441-001

**Introduction:** Lab 1 is an introduction to lab policies and procedures. Lab 1 also introduces lab equipment, tools and hardware being used throughout the semester, including logic gates and IDL-800 digital Lab manual, Altera DE1 Design and Education Board, chip extractors and pliers.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| ***NOT*** | |  | ***XOR*** | | |
| ***A*** | ***Y (output)*** |  | ***A*** | ***B*** | ***Y (output)*** |
| *1* | *0* |  | *0* | *0* | *0* |
| *0* | *1* |  | *0* | *1* | *1* |
| ***X*** | ***X*** |  | *1* | *0* | *1* |
| ***X*** | ***X*** |  | *1* | *1* | *0* |

**Theory:** Lab 1 exercises the theory of logic gates: NOT, AND, OR, NAND, NOR, XOR. The gates should act in the following ways:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***OR*** | | |  | ***AND*** | | |  | ***NAND*** | | |  | ***NOR*** | | |
| ***A*** | ***B*** | ***Y (output)*** |  | ***A*** | ***B*** | ***Y (output)*** |  | ***A*** | ***B*** | ***Y (output)*** |  | ***A*** | ***B*** | ***Y (output)*** |
| *0* | *0* | *0* |  | *0* | *0* | *0* |  | *0* | *0* | *1* |  | *0* | *0* | *1* |
| *0* | *1* | *1* |  | *0* | *1* | *0* |  | *0* | *1* | *0* |  | *0* | *1* | *0* |
| *1* | *0* | *1* |  | *1* | *0* | *0* |  | *1* | *0* | *0* |  | *1* | *0* | *0* |
| *1* | *1* | *1* |  | *1* | *1* | *1* |  | *1* | *1* | *0* |  | *1* | *1* | *0* |

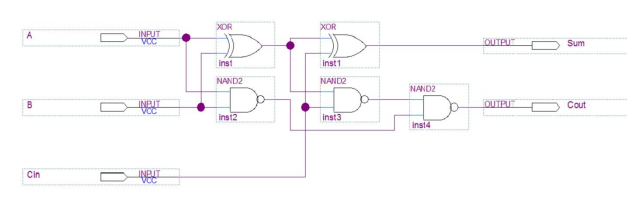
**Procedure:** Multiple chips are installed on a breadboard crossed the bridge. SN74L204 (NOT gate), SN74LS08 (AND gate), SN74LS32 (OR gate), SN74LS00 (NAND gate), SN74LS02 (NOR gate), SN74LS86 (XOR gate). The inputs of each gate is connected to the switches on the Altera DE1 Design and Education Board and the output is then connected to the LED on the same Altera board. Power is then applied to the circuit and voltage measurements are taken for logic zero and logic 1 for all gates as follows:

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***OR*** | | | | | |  | ***AND*** | | | | | |
| ***A*** | ***Va*** | ***B*** | ***Vb*** | ***Y (output)*** | ***Vy*** |  | ***A*** | ***Va*** | ***B*** | ***Vb*** | ***Y (output)*** | ***Vy*** |
| *0* | *0* | *0* | *0* | *0* | *0* |  | *0* | *0* | *0* | *0* | *0* | *0* |
| *0* | *0* | *1* | *4.94v* | *1* | *4.94v* |  | *0* | *0* | *1* | *4.94v* | *0* | *0* |
| *1* | *4.94v* | *0* | *0* | *1* | *4.94v* |  | *1* | *4.94v* | *0* | *0* | *0* | *0* |
| *1* | *4.94v* | *1* | *4.94v* | *1* | *4.94v* |  | *1* | *4.94v* | *1* | *4.94v* | *1* | *4.94v* |

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***NAND*** | | | | | |  | ***NOR*** | | | | | |
| ***A*** | ***Va*** | ***B*** | ***Vb*** | ***Y (output)*** | ***Vy*** |  | ***A*** | ***Va*** | ***B*** | ***Vb*** | ***Y (output)*** | ***Vy*** |
| *0* | *0* | *0* | *0* | *1* | *4.94v* |  | *0* | *0* | *0* | *0* | *1* | *4.94v* |
| *0* | *0* | *1* | *4.94v* | *0* | *0* |  | *0* | *0* | *1* | *4.94v* | *0* | *0* |
| *1* | *4.94v* | *0* | *0* | *0* | *0* |  | *1* | *4.94v* | *0* | *0* | *0* | *0* |
| *1* | *4.94v* | *1* | *4.94v* | *0* | *0* |  | *1* | *4.94v* | *1* | *4.94v* | *0* | *0* |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***NOT*** | | | |  | ***XOR*** | | | | | |
| ***A*** | ***Va*** | ***Y (output)*** | ***Vy*** |  | ***A*** | ***Va*** | ***B*** | ***Vb*** | ***Y (output)*** | ***Vy*** |
| *0* | *0* | *1* | *4.94v* |  | *0* | *0* | *0* | *0* | *0* | *0* |
| *0* | *0* | *0* | *0* |  | *0* | *0* | *1* | *4.94v* | *1* | *4.94v* |
| *1* | *4.94v* | *0* | *0* |  | *1* | *4.94v* | *0* | *0* | *1* | *4.94v* |
| *1* | *4.94v* | *0* | *0* |  | *1* | *4.94v* | *1* | *4.94v* | *0* | *0* |

The second part of Lab 1 is to implement a full adder using 2 XOR gates and 3 NAND gates according to the schematic:



Again the inputs A, B, and Carry in (Cin) were connected to switches on the Altera DE1 Design and Education Board and the outputs Carry Out (Cout) and Sum are connected to LEDs on the Altera board. The outputs were captured in a table and verified by the lab instructor to be correct. The calues are as follows:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| ***Full Adder*** | | | | |
| ***A*** | ***B*** | ***Cin*** | ***Cout*** | ***Sum)*** |
| *0* | *0* | *0* | *0* | *0* |
| *0* | *0* | *1* | *0* | *1* |
| *0* | *1* | *0* | *0* | *1* |
| *0* | *1* | *1* | *1* | *0* |
| *1* | *0* | *0* | *0* | *1* |
| *1* | *0* | *1* | *1* | *0* |
| *1* | *1* | *0* | *1* | *0* |
| *1* | *1* | *1* | *1* | *1* |

**Conclusion:** Overall the lab went smoothly without any problems. Next lab parts of the labs that need to be checked by the instructor will be grouped together to streamline my time in the lab.